Electronic Version
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Claims

[c1] A method of forming integrated circuit device including at least one semiconductor memory array region and logic circuits including a support region including the steps as follows:
form a thick deposit of polysilicon in both the array region where word lines are located and the support region where the logic circuits are located;
then remove the thick layer of polysilicon only in the array region;then deposit a thin layer of polysilicon in both the array region and the support region;
then deposit a metallic conductor coating including at least an elemental metal layer portion over the thin layer of polysilicon; and
then forming word lines and gate electrodes in the array region and support region respectively.

[c2] The method of claim 1 wherein:
the method begins with formation of a sacrificial polysilicon layer over the array region followed by formation of a gate oxide layer over the device, and
performing the step of precleaning the device prior to the deposit of the thin layer of polysilicon.

[c3] The method of claim 2 including forming a barrier layer between the thin layer of polysilicon and the metal layer.

[c4] The method of claim 1 wherein the thin layer of polysilicon comprises amorphous silicon.

[c5] The method of claim 4 wherein the method begins with formation of a blanket sacrificial polysilicon layer over the array region followed by formation of a gate oxide layer over the device.

[c6] The method of claim 5 including forming a barrier layer between the thin layer of polysilicon and the metallic conductor coating.

[c7] The method of claim 2 wherein a gate oxide layer is formed over the device after formation of the sacrificial polysilicon layer.

[c8] The method of claim 4 wherein a gate oxide layer is formed over the device after formation of the sacrificial polysilicon layer.

[c9] The method of claim 1 wherein a capping silicon nitride layer is formed over the metal layer before forming word lines and gate electrodes in the array region and support region.

[c10] The method of claim 9 including forming the integrated circuit device on a semiconductor substrate with a polysilicon stud is in a trench in the semiconductor substrate under an electrically conductive word line with the stud being electrically insulated from the substrate by dielectric material on sidewalls of said trench and an Array Top Oxide (ATO) layer formed above the substrate aside from the polysilicon stud; and
afterforming word lines and gate electrodes in the array region and support region forming sidewall spacers on sidewalls thereof.

[c11] The method of claim 1 wherein the step of precleaning is performed prior to the step of depositing the thin layer of polysilicon in both the array region and the support region.

[c12] An integrated circuit device including at least one semiconductor memory array and a logic circuit wherein:
said memory array includes electrically conductive word lines;
said logic circuit includes an electrically conductive gate electrode of a logic transistor;
said gate electrode and said word lines are further formed by laminations of polysilicon material and a metallic conductor coating including at least an elemental metal layer portion;

said metallic conductor coating is thicker than said polysilicon material in said word lines; and
said metallic conductor coating is thinner than the said polysilicon material in said gate electrode.

[c13] The device of claim 12 wherein said polysilicon layer in said gate electrode contains laminations of a thick gate electrode layer and a thin electrode layer.

[c14] The device of claim 12 wherein said polysilicon layer in said gate electrode contains laminations of a thick gate electrode layer and a thin electrode layer; and
the polysilicon layer in the array layer comprises only the thin electrode layer.

[c15] The device of claim 12 wherein said metallic conductor coating comprises a multilayer of a barrier layer and a metal layer.

[c16] The device of claim 12 wherein:
said polysilicon layer in said gate electrode contains laminations of a thick gate electrode layer and a thin electrode layer; and
said metallic conductor coating comprises a bilayer of a WN barrier layer and a W metal layer.

[c17] The device of claim 12 wherein a capping silicon nitride layer is formed over the word lines and gate electrodes

in the array region and support regions respectively.

[c18] The integrated circuit device of claim 16 wherein:
the integrated circuit device is formed on a semiconductor substrate,
a polysilicon stud is formed in a trench in the semiconductor substrate under an electrically conductive word line with the stud being electrically insulated from the substrate by dielectric material on sidewalls of said trench;
an Array Top Oxide (ATO) layer is formed above the substrate aside from the polysilicon stud; and
sidewall spacers are formed on the word lines and gate electrodes in the array region and support region respectively.

[c19] The device of claim 16 wherein a capping silicon nitride layer is formed over the word lines and gate electrodes in the array region and support regions respectively.

[c20] The device of claim 16 wherein sidewall spacers are formed on the word lines and gate electrodes in the array region and support region respectively.